

AMENDMENT TO THE SPECIFICATION

Please insert the following heading and subheading after the title and before the first paragraph on page 1 of the English translation:

--Background of the invention

Field of the Invention--

Please insert the following subheading before the second full paragraph beginning "For the integration of low voltage logic elements and high voltage power elements into . . ." on page 1 of the English translation:

--Description of related art--

Please replace the first full paragraph on page 2 of the English translation with the following marked-up paragraph:

--Due to the higher specific volume of the created silicon dioxide compared to the polysilicon, significant compressive stress is generated in portions near the surface of the filled isolation trenches, thereby inducing an expansion of the isolation trenches and a bending of the silicon wafer as well as generation of crystalline defects in the adjacent single crystalline silicon areas, respectively. The crystalline defects impair the characteristics of the devices and result in increased defective goods, respectively. For this reason the trench areas are covered by an oxygen impermeable layer or a corresponding layer system, as is known from US-A 5 933 746. Such cap layers are also described in US-A 5 581 110, US-A 2002/0025654, JP-A 2000-183156 and JP-A 63-003429. A disadvantage of such cap layers designed in a known manner is that these layers extend above the planar surface, which entails disadvantages in the further manufacturing process. The layers form a step, which may negatively affect the formation of conductive lines extending across the step, for instance due to a reduced thickness at the line edges. Moreover, the cap layers are defined by an additional photolithographic process and are subsequently etched, that is, a photo mask has to be

formed and deposited on the wafer, and there is the risk of a lateral misalignment of the photo mask.--

Please insert the following heading before the second full paragraph beginning "It is an object of the present invention to provide a technique for forming insulation . . ." on page 3 of the English translation:

--Brief summary of the invention--

Please replace the second full paragraph on page 3 of the English translation with the following marked-up paragraph:

--When hereby [[,]] "main process steps" are referred to during the manufacturing process, this is to be understood such that these process steps are emphasized in view of the object and the invention described and claimed herein; however, other processes, such as the integration and the processing of the low voltage elements and the high voltage elements or the etching of the trench structure are not to be excluded.--

Please replace the paragraph bridging pages 3 and 4 of the English translation with the following marked-up paragraph:

--At least one of the existing isolation trenches is provided with insulation layers, which extend as vertical insulation layers into the depth of the trench, thereby reaching to the horizontal (buried) insulation layer. At the same time a horizontal insulation layer is formed on the top of the active semiconductor layer. The fill material has a deep notch or indentation, which is still located above a height level of the horizontal insulation layer. Thus, ~~also~~ a horizontal section of the deposited fill material, which not only fills the isolation trench but is also located above the horizontal insulation layer, also [[to]] forms a fill material layer in this area. Insofar, it may be said more generally that "insulation layers are formed", which comprise horizontal and vertical portions or area sections. Both types of portions are covered by filling the at least one isolation trench.--

Please replace the first full paragraph on page 4 of the English translation with the following marked-up paragraph:

--In a further process step, the fill material layer is planarized. This is a "first planarization". Subsequently, a controlled back removal, in particular a defined back etching (back etch) is performed, which concerns the fill material in the interior of the trench, that is, below the planar surface, which is formed by the horizontal portion of the insulation layer. This removal into the trench provides for a reduction of the fill height of the trench including the oxidation sensitive fill material. This removal process is also referred to as an over-removal, which extends to "a first defined depth" of the trench, in any case to far above the trench bottom and only in the upper portion, preferably above half of the trench depth or even far above this half depth (~~claims 21, 22~~). The method is thus very appropriate for particularly deep trenches (~~claims 23, 24 and 25~~), which may extend through the entire active semiconductor layer to the buried insulation layer, not only into a certain portion of the semiconductor substrate. In this way, high voltage and low voltage at different chip regions may be reliably isolated, while avoiding oxidation influences at the surface of the trench, when this trench is filled with an oxidation sensitive material. In order to incorporate in the trench or lower the cap or cover layer provided for an oxidation barrier, a removal of a portion of the insulation layers and a further removal of a further portion of the fill material are performed.--

Please replace the second full paragraph on page 4 of the English translation with the following marked-up paragraph:

--Here, the respective vertical portions of the layers are involved and meant in order to obtain a substantially identical height level of these layers in the isolation trench or achieve the same by the additional removal process. The horizontal insulation layers are also removed so that a surface of the active semiconductor layer is exposed. This over-removal, in particular, a defined over-removal, provides a volume in the trench at the upper trench edge for accommodating a cap layer that is now to be incorporated, which extends above the level of the planar surface after deposition in the form of a layer or layer system, however, the cap layer extends downwardly to the substantially equal

height level of the trench, supported by the remaining vertical layers in the trench, a fill layer and a residual insulation layer at both sides.--

Please replace the paragraph bridging pages 4 and 5 of the English translation with the following marked-up paragraph:

--After the application of this cap layer, which is initially provided in a greater extent than required in a later stage, a further planarization process is performed. This further planarization reduces the cap, representing a functional description of a layer or a layer system, by evenly removing material using for instance a mechanical chemical polishing process or a further resist planarization process in order to again expose the surface of the active semiconductor layer, cover the trench in the upward direction in an oxide inhibiting manner, in particular in the area of the trench and ~~[[the]]~~ near the trench, such that steps are avoided~~[[,]]~~ which would complicate the formation of horizontal conductive lines.--

Please replace the first full paragraph on page 5 of the English translation with the following marked-up paragraph:

--All of the described process steps are performed without an additional photolithography step; the only photo mask required is used for forming the trenches, in this case, the at least one described trench. In addition to avoiding further photo masks, there is also no requirement for aligning these further photolithography processes to each other, so that lateral misalignments of photo masks are avoided. Oxidations may no longer occur in the upper portion of the trench, thermal stress is avoided~~(claim 6)~~, or is at least significantly reduced. Further high temperature processes may follow the formation of the trench structure without a risk for generating thermal stress that would result from ~~occurring~~ oxidation processes occurring in the upper trench portion. The process performance of the wafer is enhanced so that also yield may be increased.--

Please replace the second full paragraph on page 5 of the English translation with the following marked-up paragraph:

--If a plurality of layers are used as a layer system, at least one of the plurality of layers may be formed in a special way. In this case, on the one hand, the getter capability of ions may be taken into consideration, as well as a certain coefficient of thermal expansion. The lowered cap layer of the isolation trench enables the avoidance of a mutual negative influence of circuit portions and trench portions, such as the migration of ions. A layer component may also be used for adjusting the coefficient of thermal expansion of the total system ~~(claim 2, claim 4)~~.--

Please replace the third full paragraph on page 5 of the English translation with the following marked-up paragraph:

--Particularly advantageous is the usage of silicon nitride as an oxygen impermeable cap layer ~~(claim 3)~~.--

Please replace the fourth full paragraph on page 5 of the English translation with the following marked-up paragraph:

--The product or intermediate product of the processed wafer or process wafer in the sense of an at least partially processed SOI wafer is the subject-matter of one aspect of the invention of the present application ~~claim 26. In this claim the structural features of the process wafer defined by claim 1 are claimed as a structure.~~ The skilled person is able to determine the structure of the wafer treated or processed according to the method of the present application ~~claim 1~~ so that a relation to the manufactur[[ing]]ed product of a manufacturing or production method is possible.--

Please delete the fifth and sixth full paragraphs on page 5 of the English translation as shown in the following marked-up paragraphs:

~~--Claim 28 describes in a clear language the structural features without a „process“.~~

~~An alternative method defines in a concise manner the process flow (claim 31),
respective embodiments are defined in the respective dependent claims.--~~

Please replace the first full paragraph on page 6 of the English translation with the following marked-up paragraph:

--The continuous planar surface relates to the cap layer and the neighbouring areas, which are chip regions provided for low voltage and high voltage (~~claim 7~~). The plane is formed in a planar manner and does not form steps. The cap layer lowered into the trench also forms a laterally acting electrical insulation that extends across the entire trench width, while vertical insulation layers at the trench walls in the upper area of this cap layer are not involved (~~claim 13~~). The latter insulations are formed by, for instance, thermal oxidation and are completely removed with regards to the horizontal portions in a later stage, with regards to the vertical portion [[is]] being removed only to a certain extent [[sion]] in order to provide the space for the recessed cap layer (~~claim 8, claim 10~~). The back removal is defined and thus relates to a smaller piece of the vertical portions in the trench only (~~claim 12~~). Nevertheless the removal on the trench is performed over the entire trench width between the trench walls, which are defined by the neighbouring portions of the active semiconductor layer (~~claim 10~~).--

Please replace the second full paragraph on page 6 of the English translation with the following marked-up paragraph:

--It is to be appreciated that the cap layer is dielectrically insulating. It is also [[to]] noted that the cap layer is an oxide barrier for the fill material provided below the cap layer. This cap layer is formed without a mask (~~claim 12~~).--

Please replace the third full paragraph on page 6 of the English translation with the following marked-up paragraph:

--A dielectric insulation by means of trenches is also described in US-A 2003/0013272 (Hong) or in US-A 2003/0235975 (Tran). However, in these cases the trenches or their depths terminate [[s]] in the homogenous semiconductor material, and at the end phase of the manufacturing process, a continuous planar surface corresponding to the surface level of the semiconductor wafer is typically not achieved. In the former document, the free surface ~~maintains~~ remains covered by a double layer and is not planar. In the latter

document, the trenches are used for the isolation of differently doped regions. These regions are not provided for different potentials, such as high voltage and low voltage, that is, for accommodating power elements and logic elements, so that the trenches in the prior art may have to withstand, with respect to dimensions and design, very reduced potential differences.--

Please insert the following heading before the first full paragraph beginning "The invention will be explained and supplemented by referring to embodiments . . ." on page 7 of the English translation:

--Brief description of the several views of the drawings--

Please replace the fifth full paragraph on page 7 of the English translation with the following heading and marked-up paragraph:

--Detailed description of the invention

Figure 1 illustrates an isolation trench T according to a vertical section of a a[[n]] silicon on insulator (SOI) wafer, wherein cap or cover layers 8, 9' are provided. The cap layers 8 and 9' are located on the planar surface F' of the active semiconductor layer 3, thereby producing a disadvantageous step at Fx. The insulating trench T separates two regions 6, 7 of different potentials, wherein these regions 6, 7 are depicted while the different potentials are generated during operation of a completely processed wafer ~~separates~~ separated into individual devices having the semiconductor associated therewith. In addition to the trench T₁ the buried insulating layer 2 and the two insulating layers 4a, 4b, commonly referred to as "insulating layers 4" also provide for the dielectric insulation. The planar surface F' of the active semiconductor layer 3 has at least two lateral steps according to the covered embodiment of Figure 1, thereby inducing the previously described drawback.--

Please replace the first full paragraph starting on page 8 of the English translation with the following marked-up paragraph:

--In use, the chip region 6 and the other chip region 7 are provided with low voltage and high voltage elements, respectively, which are formed after the herein described formation of the trench structure by processes for semiconductor devices that are not specifically explained herein and that are generally known. It may only be appreciated that a first potential (P1) is assigned to the chip region 6 and a second potential (P2) is assigned to the chip region 7. These chip regions 6, 7 are portions of the active semiconductor layer 3 that is preferably made of silicon.--

Please replace the second full paragraph on page 8 of the English translation with the following marked-up paragraph:

--It should be noted with respect to the former stepped trench structure shown in Figure 1 that the arrangement of the trench area T (T indicates a [[,]]"trench") and of the two potential areas P1 (region 6) and P2 (region 7) are also determined, insofar there is no difference. It is merely to be noted that the stepped cap of the prior art is made of an oxide layer 8, which covers the trench T ~~5, 4a, 4b~~ and the fill layers 4a, 5, 4b contained therein, and is additionally covered by a cap 9', which additionally covers the insulated isolation trench T, such as Si₃N₄.--

Please replace the third full paragraph on page 8 with the following marked-up paragraph:

--Using Figures 3a to 3f, a preferred method will briefly be illustrated. The isolation trench of Figure 3a, here indicated as 5a and created by etching to the buried insulating layer 2, is provided with insulating layers 4, for instance by thermal oxidation. Thereby, the trench structure of Figure 3b is obtained. After filling the trench 5a' for instance using polysilicon~~[[5,]]~~ above the planar surface 4c, thereby forming a structure according to Figure 3c, the fill material ~~[[5]]~~ is planarized and subsequently etched back in a defined manner to form fill material 5* as shown in Figure 3d.--

Please replace the fourth full paragraph on page 8 with the following marked-up paragraph:

--Thereafter a further etch back process of the insulating layers 4 including a defined over etch is performed so that the two layers 4a, 4b and the fill material 5* have substantially the same level, as is shown in Figure 3e. Next, the cap layer 9 is formed and subsequently planarized, as is shown in Figure 3f. This may be accomplished by a chemical mechanical polish process or by a resist planarization process, which are well-known and thus are not illustrated.--

Please replace the first full paragraph on page 9 with the following marked-up paragraph:

--In detail, on the one hand, the method up to now will be explained and completed. The detailed description may, on the other hand, be considered as a further embodiment of alternative methods that are capable for producing the product of Figure 2, whose real size and shape is demonstrated by Figure 4.--

Please replace the second full paragraph on page 9 with the following marked-up paragraph:

--The trench structure, ~~from which~~ one trench ~~[[is]]~~ thereof being illustrated in cross-sectional view and which is formed by means of a first mask, is not explicitly shown as a mask, only the result of the method is shown ~~only~~. The trench 5a, whose length direction extends into the depth direction of the drawing plane, has the depth ~~[[ho]]~~ h_0 as shown in Figure 3a. It separates the left area, for ~~instance~~ instance used for the high potential P1, from the right area, used for instance for the low potential P2. The isolation area T, symbolizing the trench, creates a dielectric insulation, which will be described later on. Below the chip regions 6, 7 at the end of the active semiconductor layer 3, a horizontally buried insulating layer 2 is assumed, which is provided by the start wafer, that is, an SOI wafer that additionally comprises a carrier layer 1. The buried layer 2 has already been partially opened exposed by the trench, but will again be dielectrically

~~closed~~ covered by the following process steps in order to act as a barrier for the difference in potential P1-P2.--

Please replace the fourth full paragraph on page 9 with the following marked-up paragraph:

--The two chip regions 6, 7 to be insulated remain unchanged throughout the entire sequence of Figures 3a-3f.--

Please replace the paragraph bridging pages 9 and 10 with the following marked-up paragraph:

--Next, a process step is performed to fill the trench 5a' of Figure 3b as shown in Figure 3c. This fill process is performed such that at least the one isolation trench is filled with a fill material, wherein a deepest indentation of notch 5c of a fill material layer 5', 5'' formed at the surface is located with its top surface above a level 4c that is defined by a planar surface formed by the insulating layers 4 (the horizontal portions thereof) as shown in Figure 3c. The notch 5c is not depicted in a real manner and is not true to scale, but is a symbolic representation. The deepest level of the notch 5c as a deepest point thereof has a height offset h6 with respect to the level 4c of the planar surface [[4c]] that is used as a reference plane. The filling of the isolation trench 5a' with the fill material defines a first portion 5*, which is also referred to as a vertical portion. ~~fill material~~. Two horizontal ~~fill layers~~ portions having the same fill material are indicated as 5' and 5'' that are located on respective opposing sides of the trench, that is, above the horizontal insulating layer 4a' at one side or above the horizontal insulating layer 4b' at the other side. At the trench 5a' [[5*]], the horizontal portion as fill material layer has an indentation.--

Please replace the first full paragraph on page 10 with the following marked-up paragraph:

--The thickness [[if]] of the horizontal portion 5', 5'' of the fill material layer 5 is indicated as h5 and is somewhat greater than the thickness of the insulating layers 4.--

Please replace the second full paragraph on page 10 with the following marked-up paragraph:

--The filling of the trench 5a' with fill material provides the vertical portion [[5*]] of the fill material ~~is thus performed~~ that extends beyond the planar surface 4c ~~which means an application of the fill material~~. This information, i.e., the extension beyond or above the level 4c of the surface [[4c]], is defined by the surface or plane, which has the offset [[h5]] h₅ in the height direction, ~~as shown in~~ as shown in ~~This refers to~~ Figure 3c. In an intermediate step with respect to Figure 3d that is not shown, the horizontal portions 5', 5" of the fill material layer 5 are planarized, that is, material is removed, such that the insulating layers, i.e., their horizontal portions 4a', 4b', are again exposed. This is the first planarization.--

Please replace the third full paragraph on page 10 with the following marked-up paragraph:

--Subsequently, a defined back-removal process, in particular in the form of a back etch process, is performed so as to obtain the trench structure according to Figure 3d. This removal of an upper vertical portion of the vertical portion 5* of fill material [[5*]] relates to a part of the fill material in the interior of the trench and extends to a defined depth h7. This depth extends below the previously indicated reference plane 4c, which is now defined by the exposed top surface of the horizontal portions of the insulating layer 4. The etch-back process is performed deeper than a second reference plane 4d, which is defined by the surface of the active semiconductor layer 3.--

Please replace the first full paragraph on page 11 with the following marked-up paragraph:

--An example of such a real ratio is shown in Figure 4.--

Please replace the second full paragraph on page 11 with the following marked-up paragraph:

--Thereafter, the insulating layers 4 are further etched back, wherein here the horizontal insulating layers 4a', 4b' and a part of the vertical insulating layers 4a, 4b are involved. With this etch-back process a defined over-etch of the vertical fill ~~material layer 5~~ 5* is achieved such that the three vertical layers 4a, 5* and 4b have substantially the same height level as shown in Figure 3e. This height level is obtained by the etch-back process using the measure h9 with respect to the surface 4d of the active semiconductor layer 3. The actual etch-back for ~~[[the]]~~ obtaining the result of Figure 3e relative to Figure 3d is greater, since the horizontal insulating layers 4b' and 4a' are also removed.--

Please replace the third full paragraph on page 11 with the following marked-up paragraph:

~~--It is thus removed~~ Thus, a part of the insulating layers and a part of the vertical fill layer is removed in order to obtain and form a receiving portion that is located between the trench walls and is located more deeply than the surface of the active semiconductor layer 3. This layer is exposed according to Figure 3e.--

Please replace the fourth full paragraph on page 11 with the following marked-up paragraph:

--The opening provided has a width b9 and a depth h9, the latter is referred to the surface 4d. The application of a cap layer 9 results in a filling of the opening provided ~~this deeper lying volume~~ and concurrently covers the plane 4d so that it extends above the level of the planar surface. The extension above or protrusion is to be understood in the vertical, upward direction, at the same time the cap layer extends, after forming the same on the surface 4d of the active semiconductor layer 3, in the downward direction to the substantially identical height level in the trench. The latter corresponds to the height level of the surface 4d minus h9. This intermediate step is not shown.--

Please replace the fifth full paragraph on page 11 with the following marked-up paragraph:

~~--This intermediate step is not shown. Illustrates~~ Illustrated in Figure 3f is the result of the next intermediate step, which is not shown, in which a material removing planarization is performed, for instance by a chemical mechanical polishing process or by a resist. The corresponding process result is shown in Figure 3f, wherein the opening as described ~~volume of~~ with respect to Figure 3e is filled with a cap layer 9 ~~that is indicated as to~~ result in a surface F. The active semiconductor layer 3 is also exposed. The isolation trench cap layer 9 may thus be obtained without a mask. The cap layer 9 ensures a suppression of a possible oxidation of the vertical fill material 5*, may simultaneously provide lateral insulation and extends between the trench walls without an intermediate layer of any of the two vertical portions 4a, 4b of the insulating layer 4.--

Please replace the first full paragraph on page 12 with the following marked-up paragraph:

--Not illustrated are several layers as a sequence of layers instead of the single cap layer 9 according to Figure 3f. In this case, individual layers may have specific characteristics in order to affect the expansion behaviour or the getter capability for ions.--

Please replace the second full paragraph on page 12 with the following marked-up paragraph:

--If only one cap layer 9 is provided that forms a [[,]]"cap" of the trench, this layer may be made of silicon nitride which [[. It]] is not oxygen permeable and is electrically sufficiently insulating.--

Please replace the third full paragraph on page 12 with the following marked-up paragraph:

--The adjustment of the vertical fill material 5* and the cap layer 9 provides for the avoidance of a bending of the semiconductor wafer during subsequent processes. The upper portion of the filled trench does not oxidise so that different coefficients of expansion may not occur. The adjustment of the vertical insulating layers 4a, 4b, the vertical fill ~~layer~~ material 5* and the cap layer 9 is performed in a tailored manner.--

Please replace the fourth full paragraph on page 12 with the following marked-up paragraph:

--~~Despite~~ In addition to the stability and process safety achieved, a surface F is obtained that does not contain any steps. This especially holds true for the trench and the adjacent areas.

Please replace the fifth full paragraph starting on page 12 with the following marked-up paragraph:

--It is not ~~adverse when~~ harmful if the vertical fill material 5* is electrically conductive, since the dielectric insulating layers 4a, 4b are provided. It is also not a problem that this fill layer is oxidizable, since the cap layer 9 provides a barrier with respect to oxidation in subsequent high temperature processes.--

Please replace the sixth full paragraph on page 12 with the following marked-up paragraph:

--With respect to the depth of the material removal, it has been mentioned for the transition from Figure 3c to Figure 3d that the depth of the trench is not nearly reached and the removed portion having the depth h7 and h9 represents a small volume of the vertical fill material 5*. This is a consequence of the very deep trench structure, which is designed for a high insulation capability and a relatively thick active semiconductor layer 3. The depth of the trench and the width of the trench may be combined to an aspect ratio. This aspect ratio is higher than 10:1 (depth to width), preferably higher than 15:1. In other words, a deep narrow trench is ~~meant~~ contemplated, which is clearly ~~demonstrated~~ illustrated in Figure 4.--

Please replace the paragraph bridging pages 12 and 13 with the following marked-up paragraph:

--In a similar manner, the depth of the second over-etch process has been selected to obtain Figure 3e. Also in this case the removal is not deeper than down to half of the

trench depth at most, typically and preferably significantly less deep in order to not unduly increase the thickness of the cap layer 9, see Figure 3f. A preferred measure in this case is $\frac{1}{4}$ of the trench depth or significantly less, when the trench depth corresponds to a situation as illustrated in Figure 3e or Figure 4. The trench depth in Figure 3d is selected differently, since here only the horizontal insulating layers 4a', 4b' are provided, which may have no undue affect with respect to their extension and which are illustrated in an exaggerated manner for the sake of clarity.--

Please replace the first full paragraph on page 13 with the following marked-up paragraph:

--The thickness of the cap layer 9 may be less than 1 μm .--

Please insert the heading and paragraph on the following page as an Abstract of the Disclosure as a separate page numbered page 20.